

Serializer/Deserializer Output Data Signal Duty Cycle Correction Method

Vazgen Melikyan, Arthur Sahakyan, Artak Hayrapetyan, Abraham Balabanyan, Milena Stanojlović and Grigor Zargaryan

Abstract—A method of serializer and deserializer output data signals duty cycle correction is presented in this paper. The proposed architecture produces a data signal in the output of serializer/deserializer with 50% duty cycle over PVT, which is needed to avoid data error and setup/hold time margins violations during further operation with data. The presented correction mechanism can be used in the special input/output circuits of several standards such as Peripheral Component Interconnect (PCI), Universal Serial Bus (USB), Double Data Rate (DDR) etc.

Index Terms— Duty Cycle; Clock generator; PCI; US; DDR.

I. INTRODUCTION

In high speed systems (Fig 1.) and interfaces [1], where signal pulse width is proportional with signal transition times, signal duty cycle correction is an important factor and its effects cannot be ignored. When data signals in the inputs of Serialaizer (Fig 2.) comes with different delays and duty cycles as a result in the output signal come with duty cycle far from 50%. Duty cycle is the proportion of time during which a component, device, or system is operated. The duty cycle can be expressed as a ratio or as a percentage. One of the main factors duty cycle spreading over PVT of high speed devices is rise/fall times distribution due to process variation.

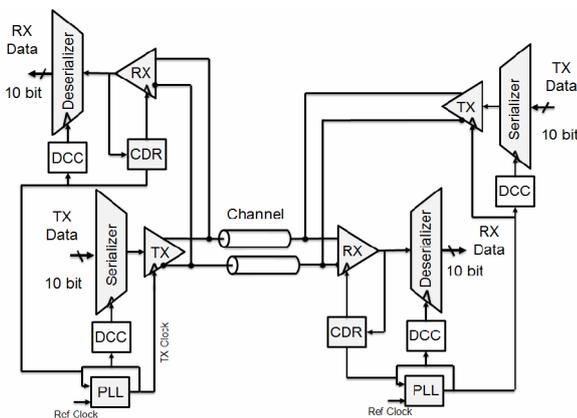


Fig.1. High Speed Serial link

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Duty Cycle Correction (DCC) [2] is required to reduce the clock signal which correcting duty cycle of the data in the output of serializer and make it near to 50%. It will cause to exclude data lost and setup/hold violations. As a result of the mentioned phenomena, the system may fail to function under some operating conditions such as high temperatures or over-voltages.

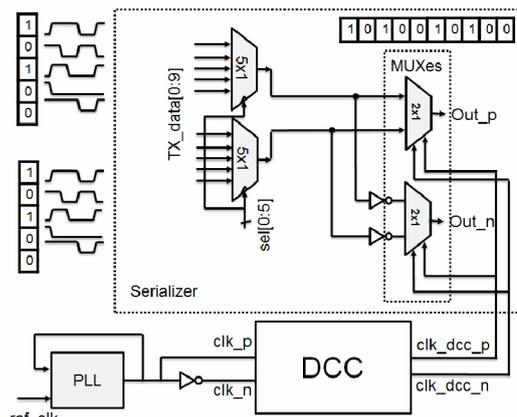
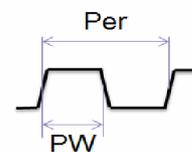


Fig.2. Serializer/DCC circuit structure

In general, the duty cycle of the wave is determined by the pulse width divided to period of signal. (1).

$$DC = (PW / Per) * 100\%. \quad (1)$$



where PW is the pulse width of signal and the Per is the period of signal. The proposed method dynamically corrected Serializer output signal duty cycle.

II. DUTY CYCLE CORRECTION CIRCUIT ARCHITECTURE

The structure of proposed Duty Cycle Correction Method is presented in Fig. 3.

In this architecture Replica part, needs corrected clocks, which dynamically fix Data signal duty cycle in the output of the Serializer. For this goal we use Replica in the loop of DCC circuit.

Correction circuit contains both analog and digital blocks.

In this structure analog blocks are Low Pass Filters (LPF), Amplifier and Clock Generator circuit (Clock Gen). Digital parts are presented with MUXes in replica DCC loop and in Serializer stage.

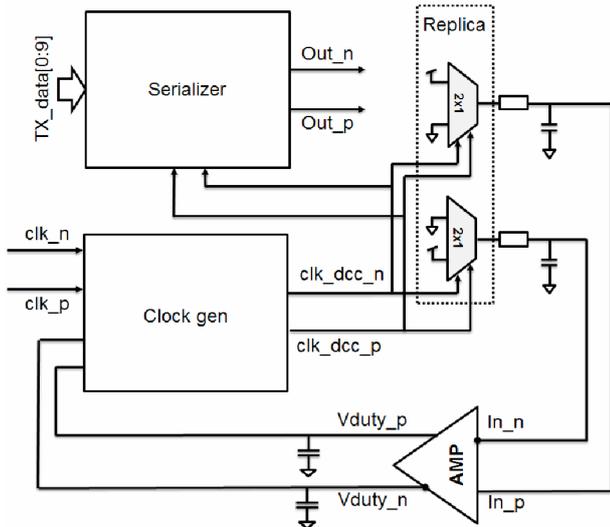


Fig.3. Duty Cycle correction circuit structure

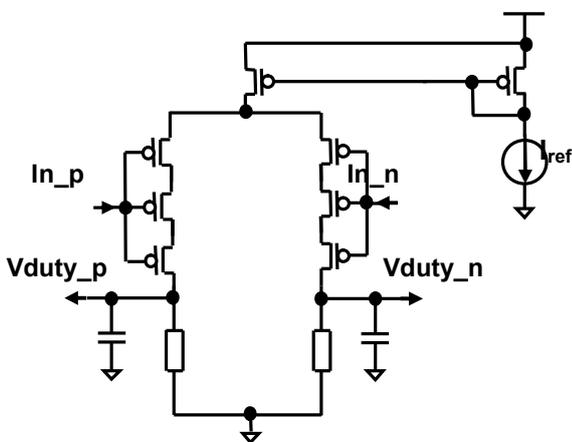


Fig.4. Delay Control Amplifier

As we need to have an amplifier that is noise stable and provides integrated voltages on the outputs depended of its inputs, we chose the following architecture in Fig 4. For that purpose the input diff pairs have large channel lengths which are implemented using sequential transistors connected with each other. To have integrated outputs capacitance loads are connected to the outputs of amplifier.

Clock Gen circuit includes voltage controllable delay cells, Desk ewer and latch. Desk ewer is used before Delay cells and proposed for skew correction and Latch is connected after Delay elements and needed for reminding current signal states unless the loop is settled. Delay elements are controlled by Diff amp outputs Vduty_p and Vduty_n

As controlled clocks are differential signals the represented MUXes are operating with 2 control inputs.

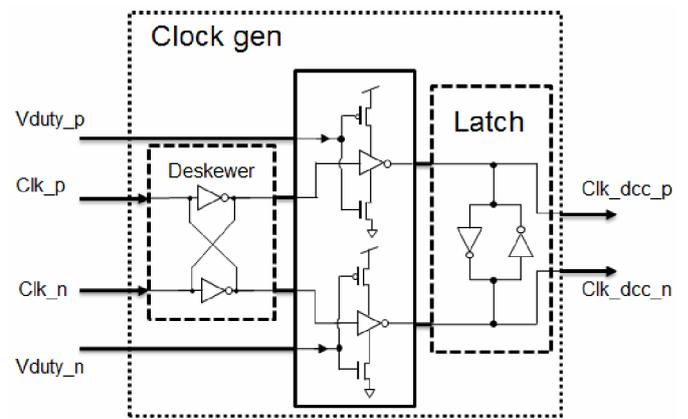


Fig.5. Clock Gen circuit structure

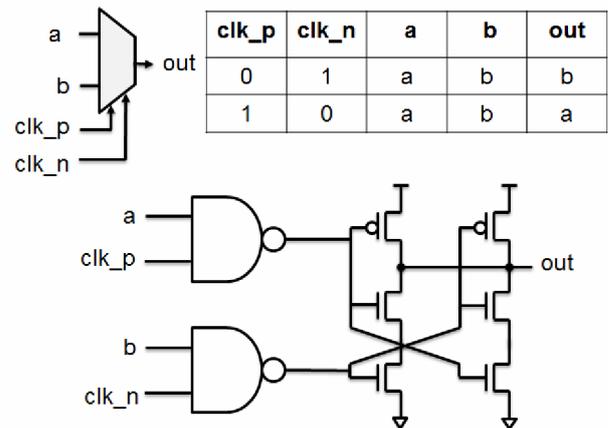


Fig.6. 2x1 MUX Serializer

III. OPERATION PRINCIPLE AND CORECTION

Block diagram on Fig 7. has been proposed to attain a duty cycle of nearly 50% for differential signals. As it is known the average DC value of a signal is proportional to its Duty Cycle. Thus it is imperative to have 50 % Duty Cycle, in order to avoid unequal distribution of '1' and '0' during signal transmission.

As it was mentioned above the clocks that are needed for serializing and deserializing data are coming from Phase Locked Loop (PLL) through lines that can affect duty cycle of these clocks over PVT.

Duty Cycle correction process starts from Clock Gen block (Fig. 5). Clock gen has 2 voltage controlled delay inverters, that are changing their output currents when Delay control amplifier changes its output voltages (Vout_p and Vout_m.). After several iterations, when loop is locked, Clock Gen generates fixed clock signals which are being used to have Serial Data with 50% Duty Cycle.

For improving Serializer output signals Duty Cycle, loop must contain Replica of Serializer. It is represented as 2x1 MUXes (Fig. 6) which inputs are connected to high and low supply voltages to have periodical data.

The output signals of Replica Serializer are passing through the LPF and so the DC component of this data is used as inputs of Delay Control Amplifier (DCA).

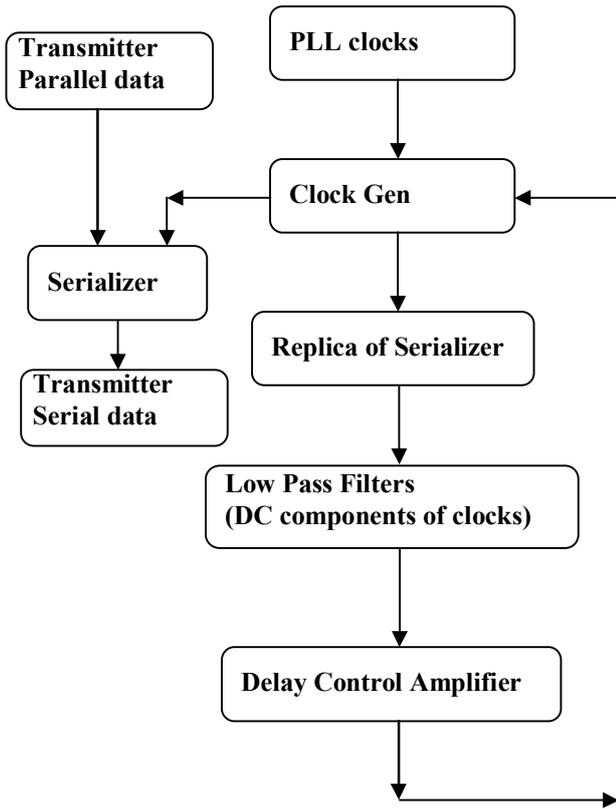


Fig.7. Block diagram of correction method

As it was said formerly the DCA input diff pair has sequentially connected transistors with large lengths and widths. Large lengths are for noise stability and large widths are for high gain. Besides as Length-Width are large enough, and taking in account the fact that external capacitor need much are, the Capacitor of LPF is implemented here using the input diff pair of DCA.

IV. SIMULATION RESULTS

Simulations have been performed using circuit level simulator HSpice [4] for 20 PVT corners, including SS (slow-slow), TT (typical-typical), FF (fast-fast), SF (slow-fast), FS (fast-slow) with supply voltage and temperature variations to estimate accuracy (Pulse width error (PWE)) and the settlement time.

Fig. 8(a) shows DCC settlement results for TT (55°) typical corner. It is seen that amplifier's outputs is going to be settled after 300ns when pulse width error is about 2.148ps. In this case $v_{dcc_p}=0.512V$ and $v_{dcc_n}=0.510V$.

Fig. 8(b) and fig. 8(c) show simulation results for, respectively, FF (-40°) and SS (125°) main PVT corners.

PWE is a parameter, which shows the difference between ideal and actual pulse widths.

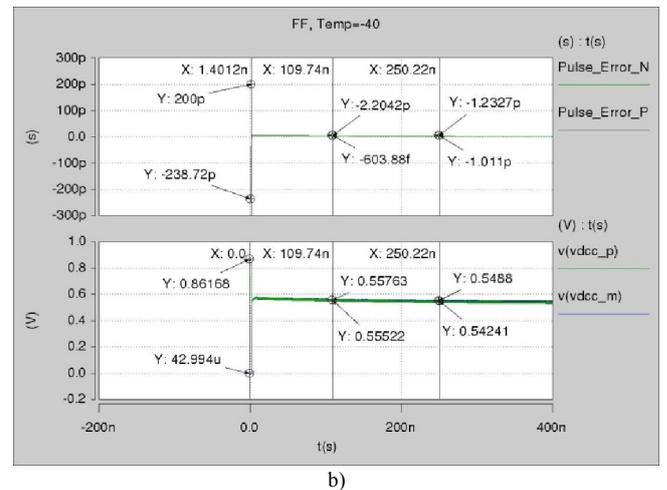
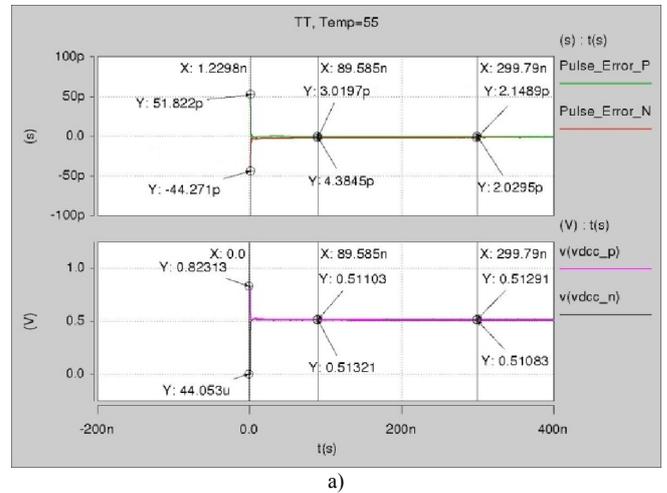
$$\text{Pulse_width_error} = \text{Pulse_ideal} - \text{Pulse_actual} \quad (2)$$

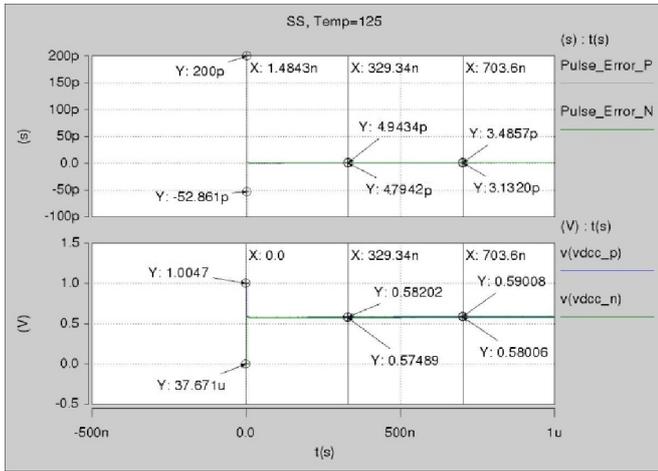
Taking into consideration that USB3 protocol works with the 5Gb/s data rate signal, which means that Data have 400ps pulse period and 200ps pulse width, we have put internal specification for PWE the 1% of period, i.e. after duty cycle can be considered as corrected, when PWE is less then 4ps. In USB3 specification book PWE min value defined as 10ps.

The next important parameter is Settling time (ST), which shows the time when Duty Cycle correction is completed. Table 1 shows results for 3 main corners.

TABLE I. SIMULATION RESULTS OF THE THREE MAIN CORNERS

Corner	PWE		Settling time
	N	P	
Unit	ps	ps	ns
TT(55)	2.0295	2.1489	299
FF(-40)	1.2327	1.011	250
SS(125)	3.1320	3.4857	703





c)

Fig.8. DCC settlement results for TT corner a) for TT (55°) b) for TT (-40°) c) for TT (1255°)

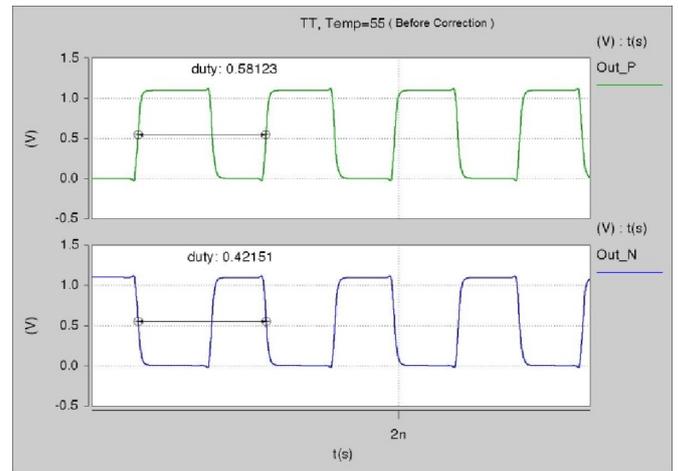
TABLE II. DUTY CYCLE CORRECTION

Corner	Duty Cycle %				Average Deviation from 50%
	before		after		
	Out_P	Out_N	Out_P	Out_N	
TT(55)	58,12	42.15	50.32	49.51	0.085
FF(-40)	55,12	43.07	50.78	49.62	0.2
SS(125)	60,24	39.35	50.13	49.25	0.62

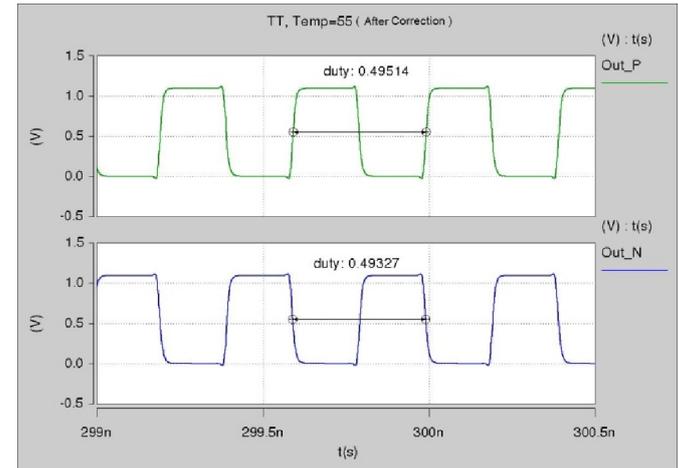
Table II shows duty cycle improvement after and before correction. Average deviation (AVED) is parameter which indicates how much duty cycle is far from 50% (3). For FF corner AVED is minimal and equal to 0.3%

$$AVED=50 \%- (DC_Out_P + DC_Out_N)/2 \quad (3)$$

Fig. 9(a) and Fig. 9(b) show simulation results before and after Duty Cycle correction for TT.



Before (a)



After (b)

Fig.9. Serializer outputs before (a) and after (b) Duty Cycle correction

V. CONCLUSION

A circuit designed for Serializer/Deserializer output data signal Duty Cycle correction. The closed loop system with negative feedback integrates data signals with skewed pulse widths and provides stable signals with corrected duty cycles.

Average Deviation for TT corner is equal to 0.085%, after 300ns of settling time; the PWE has the value of 2.1ps, whereas the spec from the USB3 specification book is 10ps.

The approached method can be implemented for input/output protocols such as USB, PCI and etc.

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